

1. A method for fabricating Salicide field effect transistors with improved borderless contacts openings comprising the steps of:
 - 5 providing a semiconductor substrate doped with a first conductive type dopant;
 - 10 forming shallow trench field oxide areas in and on said substrate surrounding and electrically isolating device areas on said substrate;
 - 15 forming a gate oxide layer on said device areas;
 - 20 depositing a conductively doped polysilicon layer on said substrate and over said device areas;
 - 25 patterning said polysilicon layer to form gate electrodes over said device areas;
 - 30 forming lightly doped source/drain areas in said device areas adjacent to said gate electrodes by ion implantation, using a second conductive type dopant;
 - 35 forming insulating sidewall spacers on the sidewalls of said gate electrodes;
 - 40 forming heavily doped source/drain contact areas in said device areas adjacent to said insulating sidewall spacers by ion implantation a second conductive type dopant;
 - 45 depositing a conformal metal layer on said substrate over said gate electrodes and said device areas;
 - 50 using a first thermal anneal to anneal said metal layer and thereby selectively forming a silicide layer

on said gate electrodes and on said source/drain contact areas;

selectively etching said remaining unreacted metal layer and thereby forming said Salicide field effect
5 transistors;

depositing a conformal etch stop layer;
depositing an interlevel dielectric layer;
etching said borderless contact openings in said
interlevel dielectric layer to said source/drain areas
10 and extending over said field oxide, wherein said
etching results in over-etched field oxide regions at
said field oxide-source/drain area interface;

ion implanting a contact dopant of said second conductive type in said borderless contact openings and in
15 said substrate under and adjacent to said over-etched field oxide regions;

using a second thermal anneal to complete the phase transition of said metal silicide and concurrently activating said ion implanted contact dopant to form
20 source/drain contact areas that are continuous around said over-etched field oxide regions.

2. The method of claim 1, wherein said semiconductor substrate is single crystal silicon.

3. The method of claim 1, wherein shallow trench isolation is silicon oxide and has a depth of between about 2500 and 4500 Angstroms and is coplanar with the surface of said substrate.

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4. The method of claim 1, wherein said conductively doped polysilicon layer has a thickness of between about 1000 and 3000 Angstroms.

10 5. The method of claim 1, wherein said metal layer is titanium and is deposited to a thickness of between about 40 and 400 Angstroms.

15 6. The method of claim 1, wherein said metal layer is cobalt and is deposited to a thickness of between about 40 and 400 Angstroms.

7. The method of claim 1, wherein said unreacted metal is removed in a solution of NH_4OH , H_2O_2 and H_2O .

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8. The method of claim 1, wherein said first thermal anneal is carried out in nitrogen at a temperature of between about 600 and 750 degrees centigrade and for a time of between about 10 and 50 seconds.

9. The method of claim 1, wherein said first conductive type dopant is a P-type dopant and said second type dopant is an N-type dopant for Salicide N-channel FETs, and the dopant types are reversed for P-channel salicide FETs.

10. The method of claim 1, wherein said second thermal anneal is carried out in nitrogen at a temperature of between about 700 and 900 degrees centigrade and 10 for a time of between about 10 and 50 seconds.

11. A method for fabricating Salicide field effect transistors with improved borderless contacts openings comprising the steps of:

15 providing a semiconductor substrate doped with a first conductive type dopant;
forming shallow trench field oxide areas in and on said substrate surrounding and electrically isolating device areas on said substrate;
20 forming a gate oxide layer on said device areas;
depositing a conductively doped polysilicon layer on said substrate and over said device areas;
patterning said polysilicon layer to form gate electrodes over said device areas;

- forming lightly doped source/drain areas in said device areas adjacent to said gate electrodes by ion implantation, using a second conductive type dopant;
- 5 forming insulating sidewall spacers on the sidewalls of said gate electrodes;
- forming heavily doped source/drain contact areas in said device areas adjacent to said insulating sidewall spacers by ion implantation a second conductive type dopant;
- 10 depositing a conformal titanium metal layer, on said substrate over said gate electrodes and said device areas;
- using a first thermal anneal to anneal said metal layer and thereby selectively forming a titanium silicide layer on said gate electrodes and on said source/drain contact areas;
- 15 selectively etching said remaining unreacted metal layer and thereby forming said Salicide field effect transistors;
- 20 depositing a conformal etch stop layer;
- depositing an interlevel dielectric layer;
- etching said borderless contact openings in said interlevel dielectric layer to said source/drain areas and extending over said field oxide, wherein said 25 etching results in over-etched field oxide regions at said field oxide-source/drain area interface;

ion implanting a contact dopant of said second conductive type in said borderless contact openings and in said substrate under and adjacent to said over-etched field oxide regions;

5 using a second thermal anneal to complete the phase transition of said metal silicide and concurrently activating the ion implanted contact dopant to form source/drain contact areas that are continuous around said over-etched field oxide regions.

10 12. The method of claim 11, wherein said semiconductor substrate is single crystal silicon.

15 13. The method of claim 11, wherein shallow trench isolation is silicon oxide and has a depth of between about 2500 and 4500 Angstroms and is coplanar with the surface of said substrate.

20 14. The method of claim 11, wherein said conductively doped polysilicon layer has a thickness of between about 1000 and 3000 Angstroms.

25 15. The method of claim 11, wherein said metal layer is titanium and is deposited to a thickness of between about 40 and 400 Angstroms.

16. The method of claim 11, wherein said metal layer is cobalt and is deposited to a thickness of between about 40 and 400 Angstroms.

5 17. The method of claim 11, wherein said unreacted metal is removed in a solution of NH_4OH , H_2O_2 and H_2O .

18. The method of claim 11, wherein said first thermal anneal is carried out in nitrogen at a temperature of
10 between about 600 and 750 degrees centigrade and for a time of between about 10 and 50 seconds.

19. The method of claim 11, wherein said first conductive type dopant is a P-type dopant and said 15 second type dopant is an N-type dopant for Salicide N-channel FETs, and the dopant types are reversed for P-channel salicide FETs.

20. The method of claim 11, wherein said second thermal anneal is carried out in nitrogen at a temperature of between about 700 and 900 degrees centigrade and for a time of between about 10 and 50 seconds.

25 21. A Salicide field effect transistors with improved borderless contacts openings comprised of:

- a semiconductor substrate doped with a first conductive type dopant and having device areas surrounded and electrically isolated shallow trench field oxide areas;
- 5 a gate oxide layer on said device areas, and a conductively doped patterned polysilicon layer second conductive type dopant over said device areas for gate electrodes;
- 10 *✓* lightly doped source/drain areas with said second conductive type dopant in said device areas adjacent to said gate electrodes and an insulating sidewall spacers on the sidewalls of said gate electrodes;
- 15 heavily doped first source/drain contact areas composed of said second conductive type dopant in said device areas adjacent to said insulating sidewall spacers
- 20 a silicide layer on said gate electrodes and on said source/drain contact providing said Salicide field effect transistors;
- 25 a conformal barrier layer, and an interlevel dielectric layer on said Salicide field effect transistors;
- 30 borderless contact openings in said interlevel dielectric layer and said barrier layer to said

source/drain areas and extending over said field oxide with unintentional over-etched field oxide regions at said field oxide-source/drain area interface;

50 a dopant composed of said second conductive type in
said substrate under and adjacent to said over-etched
field oxide regions in said borderless contact
openings providing said source/drain contact areas
with a continuous doped region around said over-etched
field oxide regions.

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22. The structure of claim 21, wherein said semiconductor substrate is single crystal silicon.

15 23. The structure of claim 21, wherein said silicide layer is titanium silicide.

24. The structure of claim 21, wherein said silicide layer is cobalt silicide.

20 25. The structure of claim 21, wherein said first conductive type dopant is a P-type dopant and said second type dopant is an N-type dopant for Salicide N-channel FETs, and the dopant types are reversed for P-channel salicide FETs.